TITLE

# HIGH-SPEED RECEIVER FOR HIGH I/O VOLTAGE AND LOW CORE VOLTAGE

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates in general to semiconductor memory. In particular, the present invention relates to peripheral circuitry for high-speed receivers connected to high I/O voltages.

### Description of the Related Art

An input-output (I/O) signal to a semiconductor device is usually a small amplitude signal within a large DC voltage range. In order to accommodate the high DC voltage, thick oxide devices are used. The receiving circuits comprising thick oxide devices to form amplifying stages, have limited performance because of large gate and junction capacitances. The receiving circuits comprising thin oxide devices to form amplifying stages and process high voltage I/O signals, are complicated circuits requiring special circuit techniques to ensure that the thin oxide devices avoid high voltage stress. Receiving circuits that transform signals from a high I/O voltage (VDDQ) to a low core (internal circuit) voltage (VDD) cause large delay skew between the rising and falling edges as VDDQ and VDD are independent.

United States Patent 6,275,094 discloses a device to shift the threshold voltage in a receiver, which has both thick and thin oxide regions. The circuitry of the receiver contains a plurality of inverters and two feedback paths. United States Patent 6,181,193 discloses a high voltage tolerant CMOS input and output

interface circuit. A receiving circuit comprises a thick oxide CMOS with dual gate devices in a receiver and a driver. United States Patent 5,911,104 discloses a chip design having thick and thin oxide and forms both bipolar transistors and DMOS transistors on the same chip. A high radio frequency receiver circuit is discussed which creates high voltage control signals. United States Patent 5,786,618 discloses a high voltage charge pump and receiver on a dual gate oxide substrate. An N-isolation buried layer underlying high density and low voltage transistors define islands of arbitrary voltage on a substrate allowing the resulting circuits to operate at high voltage relative to the substrate.

## SUMMARY OF THE INVENTION

It is an object of the present invention to adjust the common mode voltage at the output of a receiver circuit to center an I/O signal around the switching point voltage of the subsequent internal circuits.

It is another object of the present invention to construct a receiver circuit from thick oxide devices and construct the subsequent circuits driven by the receiver from thin oxide devices.

It is still another object of the present invention to create a reference voltage that approximates the switching point voltage of internal (core) circuits using thin oxide devices.

It is yet another object of the present invention to control a current in the receiver circuit to be proportional to the switching point voltage of subsequent circuits driven by the

receiver circuit, and thereby center the I/O signal around the switching voltage of the subsequent circuits.

It is still yet another object of the present invention to improve the performance of an I/O receiver circuit by constructing subsequent stages driven by the I/O receiver with thin oxide devices and by reducing the rising and falling transition skew of the signal connected to the subsequent receiver stages.

To achieve the above-mentioned objects, the present invention provides a receiver circuit. A reference voltage circuit is supplied with a first power supply voltage for outputting a reference voltage that is a mid-point voltage between the first power supply voltage and ground. A reference current circuit generates a first current according to the reference voltage. A receiving circuit is supplied with a second power supply voltage higher than the first power supply voltage, including a first current source for generating a second current according to the first current, and a differential amplifier circuit for generating an output signal contained within a voltage range of the first power supply voltage and centered around the mid-point voltage of the first power supply voltage according to the second current.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIG. 1 shows a block diagram of the I/O receiver circuit coupled to an internal (core) circuit of the present invention.

FIG. 2 shows a signal within the DC operating range of the I/O circuitry.

FIG. 3 shows the output signal of the receiver circuit centered around the switching point voltage within the voltage range of the internal circuits.

FIG. 4 is a circuit diagram of the I/O receiver circuit of the present invention.

**DETAILED DESCRIPTION OF THE INVENTION**

FIG. 1 shows a block diagram of the present invention. An I/O signal Si shown in FIG. 2 is provided to the input of the receiving circuit 10. The receiving circuit 10 is formed with thick oxide transistors and outputs an amplified I/O signal Sa shown in FIG. 3 to a internal circuit (core circuit) 11 formed with thin oxide transistors. The input I/O signal Si is within a DC voltage range of OV to VDDQ as shown in FIG. 2. The amplified I/O signal Sa produced at the output of the receiving circuit 10 is centered around a switching point voltage Vsw of the internal circuit 11 and falls within the DC voltage range of OV to VDD as shown in FIG.3.

A reference voltage Vref is generated by a reference voltage circuit 13 formed by thin oxide transistors with the same manufacturing parameters as transistors used in the internal circuit 11. Here, the voltage VDD shown in FIG. 3 is provided to the reference voltage circuit 13 and the value of the reference voltage Vref generated by the reference voltage circuit 13 is centered around the value of half VDD, close to voltage Vsw.

Thus, the switching point voltage Vsw of the internal circuit 11 is tracked by the reference voltage Vref. The reference voltage Vref is transformed to the reference current Iref proportional to the reference voltage Vref. The reference current circuit 14 is formed from thick oxide devices similar to those used in the receiving circuit 10. A current is established within the receiving circuit 10 by means of a current mirror or equivalent circuitry. The current in the receiving circuit produces a DC voltage at the output of the receiving circuit 10 around which the amplified I/O signal Sa is centered. Thus the receiving circuit 10 tracks the switching point voltage Vsw of the internal circuit 11 and balances the raising and falling delay of the amplified I/O signal Sa to improve performance of the receiving circuit 10. Here, the switching point voltage Vsw represents a threshold voltage of the transistors in the internal circuit.

FIG. 4 shows a circuit diagram of the receiver system according to the embodiment of the present invention. The reference voltage circuit 13 comprises a PMOS transistor 43 and a NMOS transistor 44 having the same p/n ratio as the transistors in the internal circuit 11. Thus, a reference voltage Vref, which is approximately VDD/2, is produced in reference voltage circuit 13, for example, a voltage divider. It is noted that the voltage VDD is lower than the voltage VDDQ. In addition, the voltage divider is formed from thin oxide devices and between internal circuit voltages VDD and VSS (ground). Because the PMOS transistor 43 and the NMOS transistor 44 are created with the same p/n ratio as transistors in the internal circuit 11 and are also supplied voltages between internal circuit voltages VDD and VSS, the reference voltage Vref generated by the voltage divider

closely tracks the switching point voltage Vsw of the internal circuits 11, which is approximately VDD/2. Here, the gates of the PMOS transistor 43 and the NMOS transistor 44 are connected to the drains of the PMOS transistor 43 and the NMOS transistor 44. In addition, the reference voltage Vref is coupled to a reference current circuit 14 comprising a resistor R3, an adjustable current source 48 and a comparator circuit 46. The comparator circuit 46 comprises a reverse input terminal, a non-reverse input terminal coupled to the gates of the PMOS transistor 43 and the NMOS transistor 44, and an output terminal. The resistor R3 is coupled between the reverse input terminal of the comparator circuit 46 and VSS (ground). The current source 48 is coupled between VDDQ and the resistor R3 for generating the current I1 flowing through the resistor R3 and generating the mid-point voltage at the connection point of the resistor R3 and the reverse input terminal of the comparator circuit 46.

Here, the comparator circuit 46 adjusts the current source 48 to make the voltage drop across the resistor R3 equal to reference voltage Vref, which is close to the mid-point voltage Vsw.

A differential amplifier circuit 40 comprises an adjustable current source 49, thick oxide PMOS transistor input pair and two resistor loads R1 and R2, having the same resistance (R/k). The PMOS transistor 41 comprising a source coupled to the current source 49, a gate coupled to an I/O signal I/O, and a drain. The PMOS transistor 42 comprises a source coupled to the current source 49, a gate coupled to a reverse I/O signal *I/O, and a drain. The resistor R1 is coupled between the connection point of the drain of the PMOS transistor 41 and the internal circuit, and VSS (ground). The resistor R2 is coupled between the

connection point of the drain of the PMOS transistor 42 and the internal circuit, and VSS (ground). The current I2 ($2 \cdot k \cdot I1$) of the differential amplifier circuit 40 is referenced to the reference current I1 of the reference current circuit 14 by a current mirror or equivalent circuitry. For example, parameter k can be "2" thus the current I2 is double the current I1.

The differential amplifier circuit 40 receives a differential signal I/O at inputs A and B. The output signal Sa of the differential amplifier circuit 40 is developed across the resistor loads R1 and R2 in both legs of the differential amplifier circuit 40 and are coupled to thin oxide devices of the core (internal) circuit 11. Here, the voltage level of the output signal Sa of the differential amplifier circuit 40 is clamped to $(2 \cdot k \cdot I1) \cdot (R1/k) = 2Vsw = VDD$ and the middle point of that is always at Vsw=VDD/2. The output signal Sa of the differential amplifier circuit 40 comprises the sum of a voltage Vref created by the current I2 flowing through the two resistors R1 and R2 of the differential amplifier circuit 40 and the amplified I/O signal as shown in FIG.3. Since the rising and falling transitions of the output signal Sa of the differential amplifier circuit 40 are centered around the switching point of the internal circuits 11, the performance of the switching of the internal circuit 11 is improved. Thus, the rising/falling delay skew of the amplified I/O signal Sa is dramatically reduced.

Accordingly, the high-speed receiver for high I/O voltage and low core voltage of the present invention combines thick and thin oxide devices to make the circuits compact and meet high input common mode voltage and speed requirements, and the signals output to thin oxide devices are clamped to core voltage to avoid high voltage stress.

The foregoing description of the invention has been presented for purposes of illustration and description. Obvious modifications or variations are possible in light of the above teaching. The embodiments were chosen and described to provide the best illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.